High Efficiency Full Bridge Current-Fed DC-DC Converter for a Fuel Cell Power System

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Abstract. A new active clamp current-fed full bridge isolated DC-DC converter topology for fuel cell applications is presented. Comparison results show that this topology improves the efficiency over a wide load range. Using small signal analysis the AC equivalent circuit and transfer functions have been derived. These show that the dynamic response for the proposed converter is more benign than that of other configurations, which will be beneficial when operating a fuel cell on a common DC bus system.

Keywords

Fuel cell, current-fed converter, small-signal analysis, zero voltage switching (ZVS).

1. Introduction

In general, DC-DC converter can be classified as non-isolating and isolating. When a fuel cell (FC) generator is interfaced with a high voltage DC busbar, galvanic isolation from the busbar or the grid is required. Also floating electrodes of the FC may cause problems especially if cells are connected in series in the stack. Compared to the DC bus voltage level (650-700V), the Proton Exchange Membrane (PEM) FC output voltage is only about 26-48V and hence the DC-DC converter must achieve by high boost ratio which may be difficult to accomplish by non-isolated converters. Therefore, the DC-DC converter usually incorporates a high frequency (HF) transformer. DC-DC converters with a HF transformer can be divided into two topologies: voltage-fed converters (VFC) and current-fed converters (CFC). CFC can be categorized into two configurations: the full bridge current-fed converter (FBCFC) [1] and the L-type current-fed converter (LTCFC) [2]. For fuel cell applications, the CFC has significant advantages over the VFC due to the lower turns ratio, higher efficiency and lower switching losses [3]. However, a CFC can cause high voltage stresses for the switching devices. Additional circuitry must be added to limit this. While the LTCFC requires less switching devices and has a lower turns ratio, it is not as the efficient as the FBCFC since it uses more passive components, requires a more complex control circuit and contains a higher input inductor ripple current.

In this paper, a new FBCFC using a voltage-doubling rectifier with untapped secondary winding and an active clamp soft switching technique is proposed. The proposed converter is described and compared with other full bridge and L-type current-fed converters in terms of efficiency and switching losses. An analysis of the proposed converter is performed to identify the periodical behaviour of the new configuration during the different modes of operation. From this a small-signal equivalent circuit has been derived which is then used to find the dynamic transfer functions.

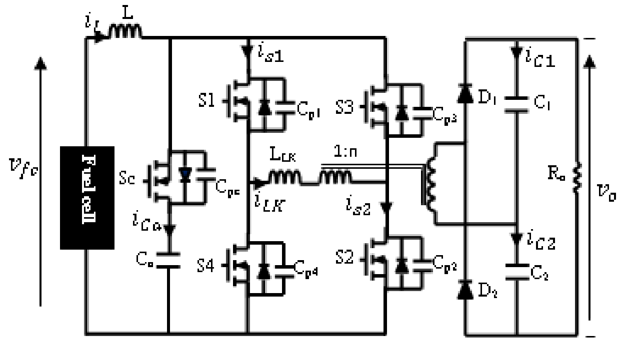
2. Steady State Analysis and Operational Modes of the Proposed Converter

The proposed CFC, shown in Fig.1a, uses a full bridge, an HF transformer with untapped secondary winding and a voltage-doubling rectifier. Using a single switch active clamp circuit, the converter alleviates the usual voltage ringing across the bridge switches. The working of this converter can be understood from analysis of the voltage and current waveforms, depicted in Fig.1b, where eight operational modes per half cycle can be distinguished:

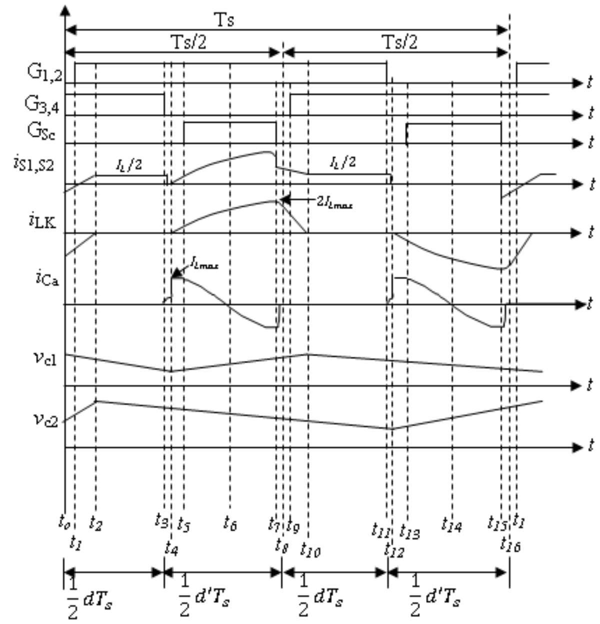
Mode 1 ($t_0< t <t_1$) zero voltage switching (ZVS) for S_1 and S_2: In this interval the anti-parallel diodes of S_1 and S_2 conduct and therefore S_1 and S_2 can be turned on with zero voltage. At this moment, the voltage across clamp branch $v_{BR}(t)$ is zero and the blocked voltage for S_c equal to clamp capacitor voltage V_{ca}. Parasitic capacitances C_{p1} and C_{p2} will be discharged at this instant. In this mode, the leakage inductance current $i_{LK}(t)$ and the anti-parallel diode current $i_{Ds1}(t)$ can be described by the following equations:

$$i_{LK}(t) = i_{LK}(t_0) - \frac{V_{Ca} - V_o/2n}{L_{LK}}(t - t_0) \tag{1}$$

$$i_{Ds1}(t) = i_{LK}(t_0) - \frac{V_{Ca} - V_o/2n}{L_{LK}}(t - t_0) - i_L(t) \tag{2}$$



(a) New FBCFC configuration



(b) Voltage and current waveforms, showing operational modes

Fig. 1. Proposed active clamp FBCFC with voltage doubler

Mode2 (t_1< t <t_2) S_1 and S_2 turn on: In this mode, S_1 to S_4 will all be conducting and the current in each leg increases to half the boost inductor current $i_L(t)$. The leakage inductance current is described by:

$$i_{LK}(t) = I_L - \frac{V_o/2n}{L_{LK}}(t - t_1) \tag{3}$$

Mode3 (t_2< t <t_3) overlap interval: In this interval, S_1-S_4 are turned on and no energy is transferred through the transformer; the output capacitors (C_1 and C_2) will sustain the load. At this interval $i_{LK}(t)$ is zero.

Mode 4 (t_3< t <t_4) charging parasitic capacitors of S_3 and S_4: At t = t_3 S_3 and S_4 are turned off and each half of input current $i_L(t)$ charges the parasitic capacitors C_{p3} and C_{p4} to the clamp voltage $v_{ca}(t)$ at t_4, thus limiting the voltage across the bridge switches. In addition, $v_{sc}(t)$ reduces to zero resulting in a discharge of the parasitic capacitor C_{pc} and charging of the clamp capacitor C_a. At t = t_4 C_{p3} and C_{p4} are full charged and $i_{Cp3}(t)$ and $i_{Cp4}(t)$ will be zero. Also, C_{pc} is fully discharged and its current is zero. At t_4 $i_{Ca}(t)$ will be equal to I_{Lmax}. The clamp branch voltage $v_{BR}(t)$ and the voltage across C_{pc} can be described by the following equations:

$$v_{BR}(t) = v_{Cp3}(t) = V_{Ca}(t - t_3) \tag{4}$$

$$v_{Cpc}(t) = V_{Ca} - V_{Ca}(t - t_3) \tag{5}$$

Mode5 (t_4< t <t_5) anti-parallel diode of S_c conducts: At t = t_4 the current $i_{Ca}(t)$ will be equal to I_{Lmax} and the leakage current is given by the following equation:

$$i_{LK}(t) = \frac{V_{fc} - V_{Ca}}{L} - \frac{V_{fc} - V_{Ca}}{L}\cos\left(\omega_o(t - t_4)\right) \tag{6}$$

$$v_{Ca}(t) = V_{Ca} + I_L Z_o \sin\left(\omega_o(t - t_4)\right) \tag{7}$$

where $\omega_o = 1/\sqrt{(L_{LK}C_a)}$ is the resonant frequency and $Z_o = \sqrt{(L_{LK}/C_a)}$.

A resonant energy exchange now takes place between L_{LK} and C_a until t = t_7 : From t_5 to t_6 the difference between $i_{LK}(t)$ and $i_L(t)$ flows into C_a via the anti-parallel diode, until the current reverses sign.

Mode 6 (t_5< t <t_6) S_c turned on: Due to the discharge of C_{pc} the anti-parallel diode of S_c is conducting resulting in zero voltage across S_c at t = t_5. This allows S_c to turn on under ZVS. The same equations as for Mode 5 will hold.

Mode 7 (t_6< t <t_7) transfer energy: At t_6 the $i_{Ca}(t)$ equal to zero and then energy stored in it starts to transfer into the primary winding in a resonant fashion started in mode 5. At t = t_7, $i_{ca}(t)$ will have the same value as $i_L(t)$ but with the opposite sign. The currents in S_1, S_2 and L_{LK} are then equal to approximately twice the input current at t_7. S_c is now turned off.

Modes 8, 9 &10 (t_7< t <t_{10}) L_{LK} discharging period: At t = t_7 S_c is turned off while S_1 and S_2 remain on. At this instant the current via S_1 and S_2 will be 3/2 times the boost inductor current and $i_{LK}(t)$ is still greater than input current. Turn-off of S_c stops the main discharge of C_a and another resonant process between C_{p3}, C_{p4}, C_{pc} and L_{LK} take places that can be described by

$$i_{LK}(t) = 2I_L - \frac{V_{Ca} - V_o/2n}{L_{LK}}(t - t_7) \tag{8}$$

$$v_{BR}(t) = V_{Ca} - I_L Z_o \sin\left(\omega_o(t - t_7)\right) \tag{9}$$

Some discharging of C_a continues until the voltage across C_{pc} becomes negative, but C_{p3} and C_{p4} are being reverse-charged by the leakage inductance energy until the anti-parallel diodes of S_3 and S_4 start to conduct (t_8). This creates a ZVS condition for these devices, which then switched on at t_9. At t_{10} $i_{LK}(t)$ has fallen to zero and the switch currents are again equal to 1/2 of the input current. Modes 9 to16 are similar to modes 1 to 8 but differ in the way the output capacitors C_1 and C_2 are being charged.

3. Comparison of the proposed CFC with other CFC topologies

Operation of different current-fed converters configurations, suitable for fuel cell power systems, has been analyzed and compared with the proposed FBCFC. To achieve a fair comparison, all converters topologies are designed to the same specifications as listed below.

Fuel cells stack characteristics:

- Maximum output power = 1.2kW
- FC voltage = 26-50 V
- Maximum FC ripple current ≤35%.

Converter characteristics;

- Switching frequency = 50kHz
- DC bus voltage = 650V

The calculated components values are listed in Table1.

Table 1 Calculated component values for four CFC topologies

Topology	C_a, µF	L_{lk} µH	L_1 µH	L_2 µH	n	C_o µF
Tapped-transformer FBCFC[4]	-----	2.5	500	-------	1:6	250
Proposed FBCFC	1.92	1.5	500	-------	1:6	100
Active clamp LTCFC[5]	1.92	1.5	500	500	1:6	250
Voltage doubler LTCFC	2.88	1	500	500	1:3	100

The main waveforms of the hard switched voltage doubler FBCFC using a tapped transformer [4] are shown in Fig. 2.

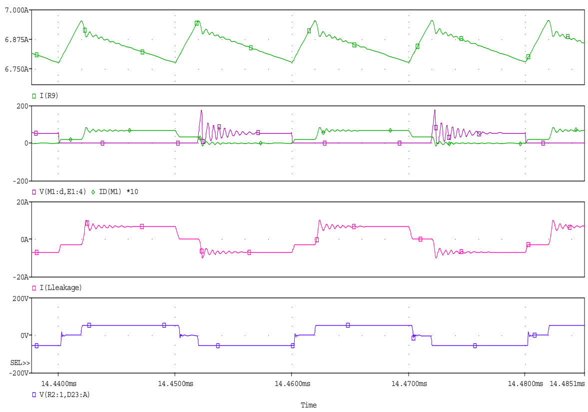


Fig.2 Voltage and current waveforms of hard switched FBCFC with voltage doubler [4]

From this figure, it is noted that there is severe ringing of the voltages across the switches to twice the reflected output voltage. On the other hand, as can be seen from the analysis results of the proposed converter in Fig.3, the voltage across the switches is clamped by clamp circuit.

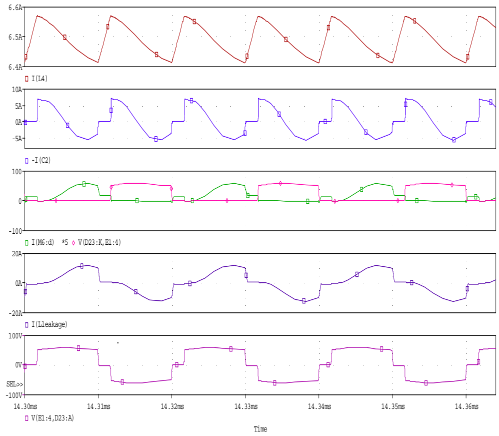


Fig.3 Voltage and current waveforms of the proposed FBCFC

Fig.4 illustrates that the proposed converter exhibits a much improved efficiency over the entire load range (up to 97% at 60 percent of the full load) compared with other topologies.

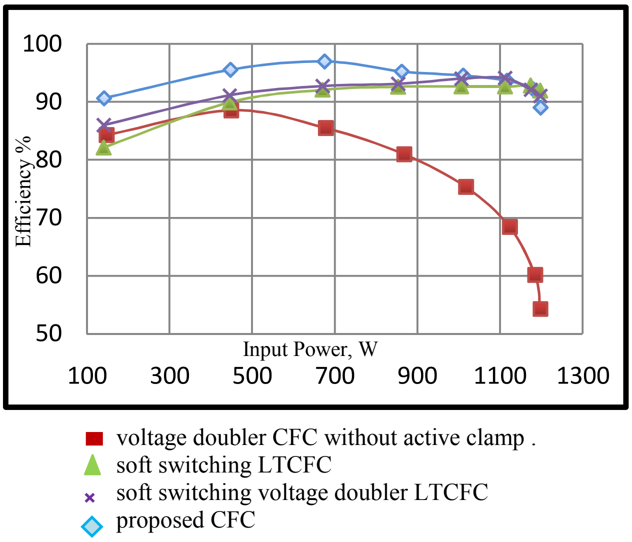


Fig.4 Efficiency comparison of four CFC configurations

Table.2 gives a detailed comparison of the power losses incurred in the different topologies and also demonstrates the lower device stresses for the proposed converter.

2. Small Signal Equivalent Circuit and Transfer Functions of the Converter

The dynamic equations for the boost inductor voltage $v_L(t)$, leakage inductor voltage $v_{LK}(t)$, clamp capacitor current $i_{ca}(t)$, output capacitor currents $i_{c1}(t)$ and $i_{c2}(t)$ have been derived for each mode. After that, the small signal approximation is achieved by replacing the voltage and currents with their average values, while averaging voltages and currents over one switching cycle. The nonlinear set of differential equations is then perturbed and lineraized to construct the small signal equations. These equations contain DC terms, 1st order linear AC terms and 2nd order nonlinear AC terms. By neglecting

Table 2. Comparsion of the proposed FBCFC with other toplogies

Parameters	**FBCFC with tapped-transformer**	**Proposed FBCFC**	**Active clamp LTCFC with full bridge rectifier**	**voltage doubler LTCFC**
Total switching loss/switch, W	10.1	1.37	5.83	6.04
Total switching loss/clamp switch, W	-----	0.89	1.9	1.27
Total switching loss, W	40.4	6.37	15.46	14.62
Total Conduction loss, W	40.7	22.08	17.23	15.8
Total loss, W	81.1	28.45	32.69	30.42
Peak current in $L_{leakage}$, A	21.13	30.5	15.8	14.9
RMS current in $L_{leakage}$, A	13.23	17.1	8.5	8.3
Peak current in main switch, A	18.74	30.54	24.3	23.27
RMS current in main switch, A	10.65	12.67	11.26	11.17
Peak current in clamp switch, A	-----	14.4	8.3	10.16
Input ripple current%	1.84	1.84	3.38	2.96
Inductor ripple current%	1.84	1.84	12.9	13.2
Inductor current frequency	2*f_s	2*f_s	f_s	f_s
Input current frequency	2*f_s	2*f_s	2*f_s	2*f_s
Input ripple current%	1.84	1.84	3.38	2.96
switch voltage stress, V	234.28	68.28	118.5	119.8
Efficiency%	85.5	97.0	91.7	92.2

the first term and the third term and then taking the Laplace Transform, the following small signal state space equations are obtained:

$$\begin{bmatrix} s.L & D' & 0 \\ -D' & s.C_a + g_3 & -g_2 \\ -J & -p_3 & s.\frac{C}{2} + p_2 \end{bmatrix} . \begin{bmatrix} \hat{\imath}_L(s) \\ \hat{v}_{Ca}(s) \\ \hat{v}_o(s) \end{bmatrix} = [\hat{d}(s)]. \begin{bmatrix} V_{Ca} \\ g_1 \\ -p_1 \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} [\hat{v}_{fc}(s)] \quad (10)$$

where

$$g_1 = \frac{D'\left(V_{Ca} - \frac{V_o}{2n}\right)}{2L_{LK}f_s} - I_L \quad (11)$$

$$J = \frac{2(D' + D'')}{n} \quad (12)$$

$$p_2 = \frac{JI_L}{V_o} + \frac{1}{R_o} \quad (13)$$

D', g_2, g_3, p_1 and p_3 are equal to (1-D), $D'^2/(8nL_{LK} f_s)$, $D'^2/(4L_{LK} f_s)$, $(4I_L V_{Ca})/V_o$, and $(4I_L D')/V_o$ respectively and D'' is a period of energy transfer from L_{LK} to the load.

From (10) the Control-to-output voltage transfer function and small-signal trenasfer function for duty cycle-to-boost inductor current can be derived as shown in (14) and (15) respectively:

$$G_{vd}(s) = \left.\frac{\hat{v}_o(s)}{\hat{d}(s)}\right|_{\hat{v}_{fc}(s)=0} = G_{g0}\frac{m_1 s^2 + m_2 s + 1}{q_1 s^3 + q_2 s^2 + q_3 s + 1} \quad (14)$$

$$G_{id}(s) = \left.\frac{\hat{\imath}(s)}{\hat{d}(s)}\right|_{\hat{v}_{fc}(s),\hat{v}_o(s)=0} = G_{i0}\frac{a_o s + 1}{b_1 s^2 + b_2 s + 1} \quad (15)$$

where

$$\boldsymbol{G_{g0}} = \frac{\boldsymbol{-p_1 D'^2 + J g_3 V_{Ca} - J D' g_1 + p_3 V_{Ca} D'}}{\boldsymbol{p_2 D'^2 + J g_2 D'}} \quad (16)$$

$$m_1 = \frac{-L.C_a.p_1}{-p_1 D'^2 + J g_3 V_{Ca} - J D' g_1 + p_3 V_{Ca} D'} \quad (17)$$

$$m_2 = \frac{C_a J V_{Ca} - g_3 p_1 L + p_3 g_1 L}{-p_1 D'^2 + J g_3 V_{Ca} - J D' g_1 + p_3 V_{Ca} D'} \quad (18)$$

$$q_1 = \frac{L.C.C_a}{2p_2 D'^2 + 2J g_2 D'} \quad (19)$$

$$q_2 = \frac{L.C.g_3 + 2C_a L p_2}{2p_2 D'^2 + 2J g_2 D'} \quad (20)$$

$$q_3 = \frac{D'^2 C - 2g_2 p_3 L + 2p_2 g_3 L}{2p_2 D'^2 + 2J g_2 D'} \quad (21)$$

$$\boldsymbol{G_{i0}} = \frac{\boldsymbol{g_3 V_{Ca} - g_1 D'}}{\boldsymbol{D'}} \quad (22)$$

$$\boldsymbol{a_o} = \frac{\boldsymbol{C_a . V_{ca}}}{\boldsymbol{g_3 V_{Ca} - g_1 D'}} \quad (23)$$

where b_1 and b_2 are equal to (LC_a / $\boldsymbol{D'^2}$) and (L /$4L_{LK}f_s$) respectively**.**

A small signal equivalent circuit that corresponds to the above state-space equations is depicted in Fig.5.

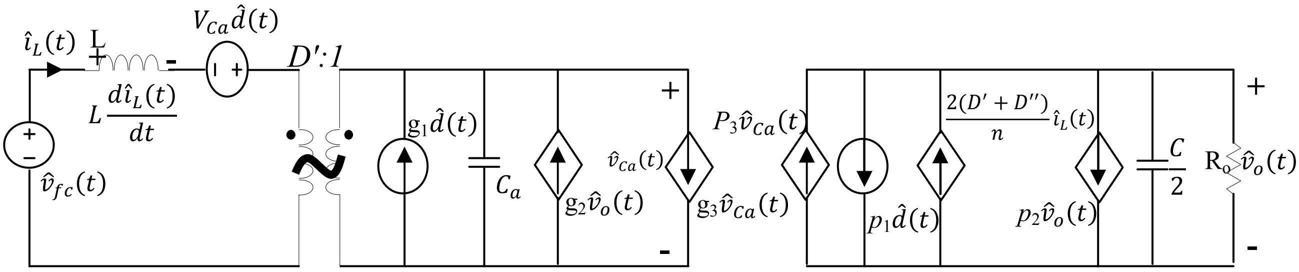
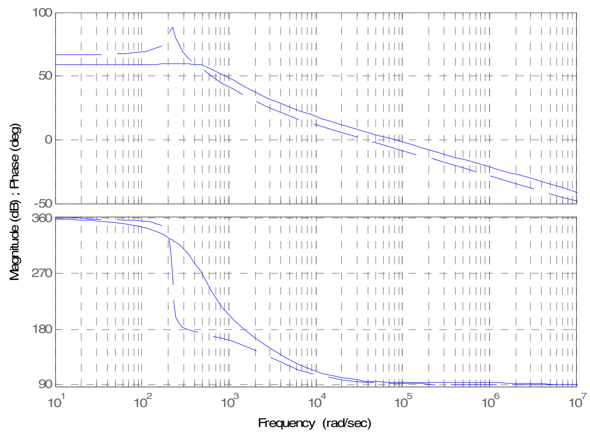
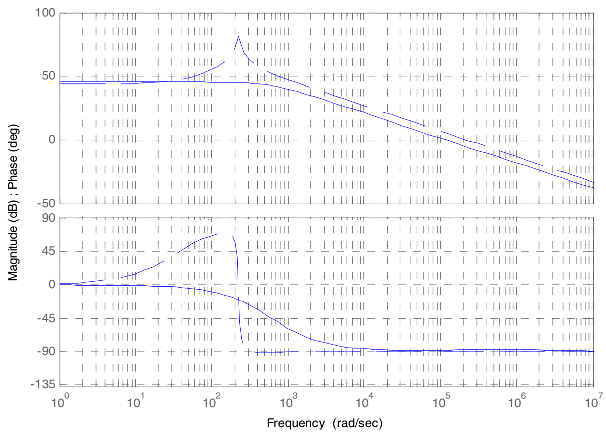


Fig.5. Small-signal AC equivalent circuit

The Bode plots of G_{vd} and G_{id} are shown in Fig.6 for the standard FBCFC without active clamp [4] and the proposed FBCFC, where it can be seen that the output voltage and input current do not longer contain an oscillatory mode.



(a) Bode plot of G_{vd}



(b) Bode plot of G_{id}

----- Standard FBCFC [4]
—— proposed CFC

Fig. 6 Bode plots of G_{vd} and G_{id} for FBCFC [4] and proposed CFC

3. Conclusion

The results of the comparison and dynamic modelling analysis described above show that the proposed converter operates at a very high efficiency (up to 97%), has low switch stresses, and has a higher voltage ratio compared with other CFC topologies. The latter simplifies the HF transformer construction, improves window utilization and reduces the leakage inductance. The transient response shows that the new configuration has a more benign behaviour, simplifying the design of closed loop controller and protecting the fuel cell from damaging overcurrents.

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