# Inter- Line Dynamic Voltage Restore and Fault Current Limiter (IDVR-FCL)

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**Abstract.** This paper proposes a novel combined device for fault current limiting and dynamic voltage restoring. It consists of a diode bridge superconducting fault current limiter and a dynamic voltage restorer, which both connected together via a common dc link. Interline FCL-DVR system is interlined between two different feeders that connected to a point of common coupling (PCC) in distribution network. The structure, control strategy and capability of this equipment are discussed in this paper. Effectiveness of proposed configuration is verified through simulation by PSCAD/EMTDC.

***Keywords:*** superconducting *Fault Current Limiter, Dynamic voltage restorer (DVR), voltage sag, power quality*

## 1. Introduction

Power quality problems are becoming more and more important for electric utilities due to growing of the number of sensitive loads. Sensitive loads such as computers, process industries and process control often drop off-line due to voltage sag. As a result, some industrial facilities, experience product in outage that result in tremendous economic losses [1]. Therefore utilities are currently exploring mitigation techniques that eliminate impact of voltage sag during a fault and increase the reliability of the power supply. Furthermore, voltage sag are mainly caused by faults in distribution network, so an effective fault current limitation device placed at beginning of the most exposed feeders will limit the expected voltage sag and improve the system power quality[2]. On the other hand there are new technologies like custom power devices based on power electronic converters to provide protection against power quality problems [3]. DVR is a series custom powers device designed specially to improve power quality in distribution network. The main function of a DVR is the protection of sensitive loads against voltage sag. As shown in Fig .1 the DVR is located in between the PCC and the sensitive loads. When fault occurs on other lines, DVR by injecting an appropriate

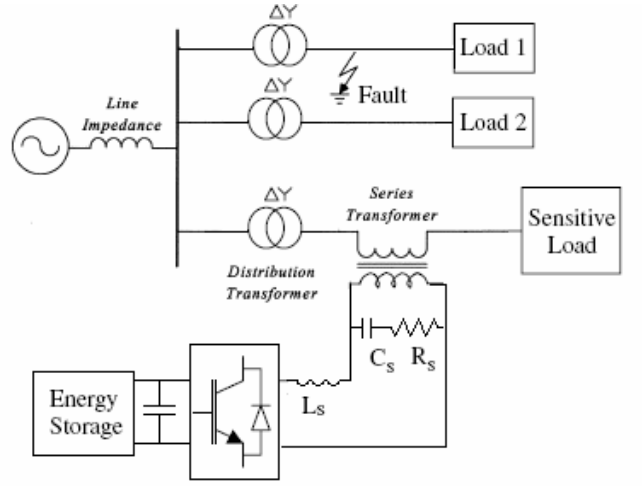



Fig. 1. Power circuit of DVR

voltage, in series and synchronism with PCC voltage, it can be restored to pre-fault value. In this paper the common diode bridge superconducting fault current limiter and a DVR has been integrated to new equipment for fault current limiting and voltage quality improving functions. When the voltage of PCC drops greatly during fault on other feeders for a long time the energy storage in DVR required high capacity superconducting coil that leaded to high cost. A major disadvantage of bridge superconducting fault current is that it can not limit the steady fault current. From this point of view combined of DVR and bridge superconducting fault current limiter(BSFCL) can not only limit the peak and steady fault current, but also protect the voltage of sensitive loads and PCC from voltage sag with just one superconducting coil, and using DVR with lower power converter rating. The other advantage of this device is using of a lower capacity of superconducting coil, compared with a single DVR and a single FCL.

## 2. Principle of operation

### *A. 3-phase diode bridge type SFCL*

The three-phase diode bridge type SFCL consists of the superconducting coil that is connected to the secondary winding of series transformer, through diode bridge circuit as shown in Fig. 2. The diode bridge performs as a rectifier converting three-phase AC to DC, which flows through the superconducting coil. At steady stage the current through SC is nearly constant, so the secondary circuits of the transformer are short circuit state. Therefore impedance seen by the primary side of the coupling transformer is very low. Under the fault conditions, the increment of fault current can be limited by inductance of SC without delay and the fault current increases gradually with a constant rate during fault[4]-[7].

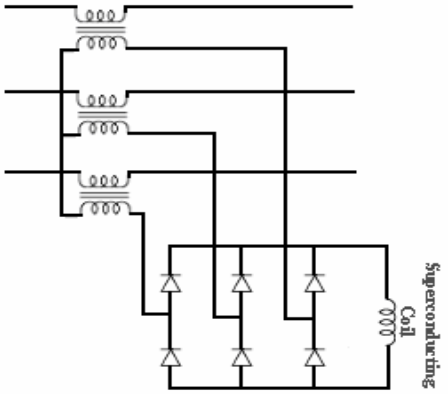



Fig. 2. Diode bridge type SFCL

### *B. Dynamic Voltage Restore(DVR)*

The DVR is a series custom power device used for protecting sensitive loads from adverse effect of voltage disturbances at the point of common coupling (PCC). The DVR essentially consist of a series connected injection transformer, a voltage source inverter (VSI), inverter output filter and an energy storage device connected to the dc link. If a fault occurs on other lines, DVR inserts series voltage and compensates load voltage to pre-fault value. As the DVR is required to inject active power in to the line during the period of compensation, the capacity of the energy storage unit can become a limiting factor in disturbance compensation process[8]-[11].

### *C. Interline DVR-FCL*

Fig. 3 shows the configuration of three phase interline FCL-DVR system. It is mainly composed of a voltage source inverter (IGBT G1-G6), a current regulator (IGBT G7-G10, MOSFET T1-T2), a superconducting coil, three phase diode bridge rectifier (D1-D6). A DC capacitor(C) is located between inverter and regulator. The VSI is connected between the power supply and load via The three boost transformer (Ta,Tb,Tc), which are its DVR function port, and DC link voltage is connected through current chopper (current regulator) to SC to maintain the voltage. Another three linking transformer (TA, TB, TC) are its FCL function port which connected via three phase diode bridge to SC. Interline DVR-FCL system can be interlined between the common and critical loads connected to PCC, and when fault occurs on one of the feeder of common loads, this system can work automatically to limit the current all along by its FCL port. One of advantage of this type is that the waveform of fault current does not have a surge current, because of SC prevents a sudden increasing of fault current. Really, the fault current increases slowly during the fault and the current of SC will rise, too and magnetic energy stored in SC will increase accordingly. At the same time, the current regulator works as controlled resistor or absorbing the energy from the SC to provide constant voltage for the capacitor.

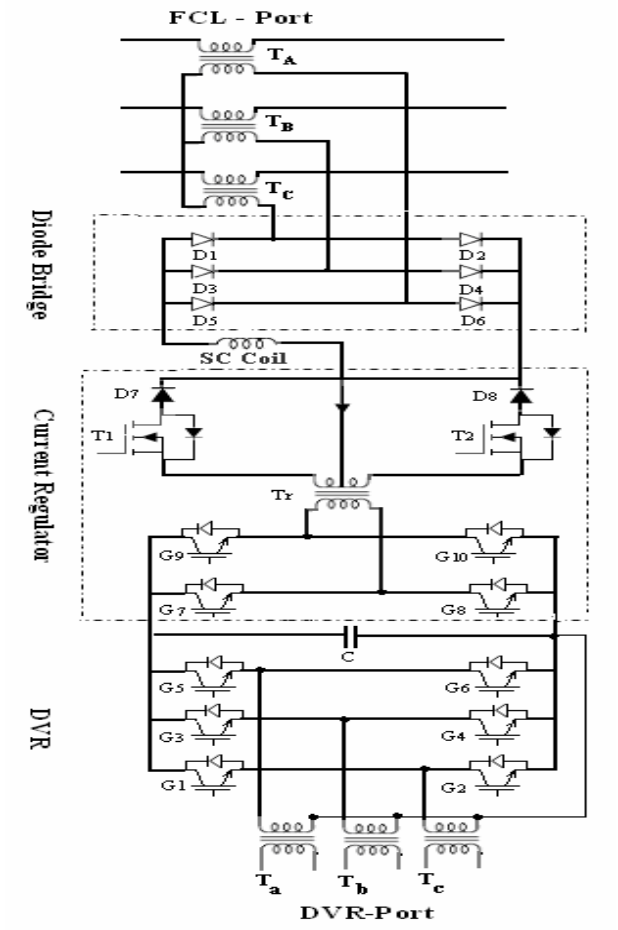



Fig. 3. Interline DVR-FCL

Then the DC voltage of capacitor is converted by voltage source inverter of DVR in to ac voltage, and injected in to the system through the linking transformer by DVR port to implement the voltage compensating function. Thus, the fault current is limited and voltage sags is also compensated, too.

## 3. Control Strategy

The main function of the DVR is to compensate the PCC voltage sags by injecting an appropriate voltage in series and in synchronism with the incoming PCC voltage, so that the load voltage (the sum of PCC voltage and insertion voltage) can be restored to its desired level. For proper operation of the DVR, the voltage at PCC is sensed. Once a PCC voltage sag is detected, the DVR is controlled with a reference voltage of $Vref=V_{PCC\_ref} - V_{PCC}$, where $V_{PCC\_ref}$ is usually obtained by a PLL locked to the pre-sag PCC voltage. The magnitude and phase of load voltage $V_{Load}$ is therefore unchanged. This compensation is known as pre-sag compensation (or voltage quality optimized compensation). The drawback is the capacity limitation of energy storage device for the injection of real power. However with combined FCL DVR solves this problem. In fact the current regulator by absorbing stored energy of the SC, which is increased by the fault, provides a constant DC voltage for the capacitor. Fig.4 shows the control scheme of the pre-sag compensation strategy. The current regulator works as interface between the DC link of voltage source inverter and SC, which kept constant the capacitor voltage. Fig. 5 shows the control scheme of current regulator [9]-[10].

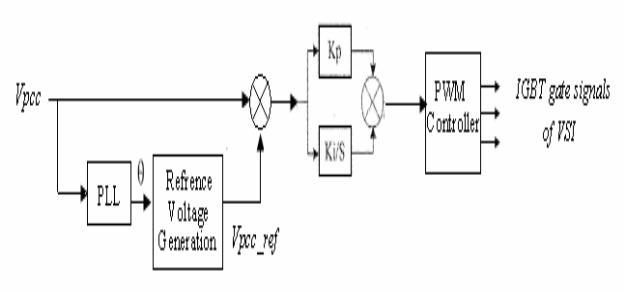



Fig .4. Control schem of the pre-sag compensation strategy

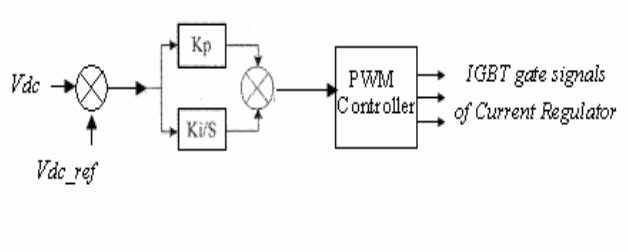



Fig.5. Control scheme of current regulator

## 4. Simulation

Simulation studies were carried out with the PSCAD/EMTDC to investigate the operational characteristic of FCL combined with the DVR. The analyses were conducted with the model shown in Fig.6 and with parameters shown in Table1. A carrier based PWM controller is used to generate gating signals of IGBTs used in the VSI Bridges of the DVR and current regulator.

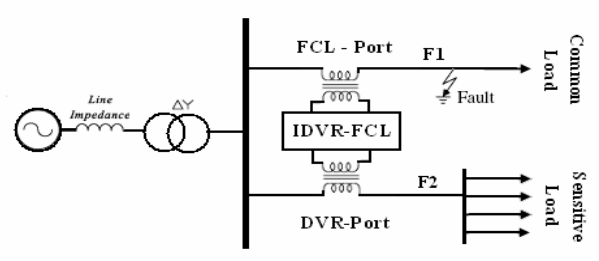



Fig. 6. Schematic diagram of the study system

TABLE I. SYSTEM PARAMETERS

| Parameter | | Value |
|---|---|---|
| **Grid** | Supply | 20KV |
| | frequency | 50Hz |
| | X/R ratio | 8 |
| | Step down transformer | 20KV/8KV 10MVA |
| **Line** | R | .1(Ω/Km) |
| | X | .2(Ω/Km) |
| | Length of F1 | 12Km |
| | Length of F2 | 8Km |
| **Load** | Common load | 1MW,pf=.8lag |
| | Sensitive load | 1MW,pf=.9lag |
| **Inter-line DVR-FCL** | transformers | 8KV/4KV,5MVA |
| | DC link capacitance | 3KV,1000uF |
| | Superconducting Coil | .1H |
| | High frequency transformer | 20KH,n=10 |

## 5. Simulation results

The first simulation is run for a symmetrical downstream fault in feeder F1 which connected to common load. The three phases of the load at low voltage side are short-circuited from 500 ms to 650 ms (lasts for 7.5 cycles). Plots 1 and 2 of Fig.7 show the line current in feeder F1 and voltage of PCC respectively without FCL and DVR. It is obvious that the downstream short circuit causes extremely high currents due to the very limited source and line impedance, which might cause damaging effects within a few cycles. The short circuit currents in plot1 of Fig.7 comprise of a dc component and symmetrical ac components. The dc component causes the short circuit current to be asymmetrical and the decay of the dc component depends on the X/R ratio of the circuit between

the source and the fault. The PCC voltages shown in plot2 of Fig.7 drop to about 50%, due to the similar leakage impedance of transformer which would provide main source and line impedance of the system. Plot 1 and plot2 of Fig.8 show line current (in feeder F1) and PCC voltage when using common bridge SFCL for limiting fault current. It can be observed from Fig.8, which the fault current does not have surge current, but fault current (in feeder F1) and voltage sag in PCC gradually increase during the fault. Therefore the sensitive loads on other feeder connected in PCC will be affected. This voltage sag in sensitive loads is more than acceptable level and power quality standard.

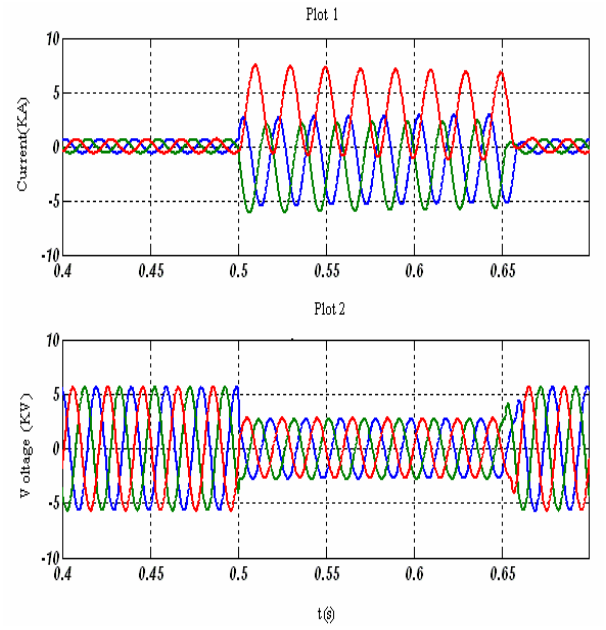



Fig.7. Currents and voltages during fault without using FCL and DVR

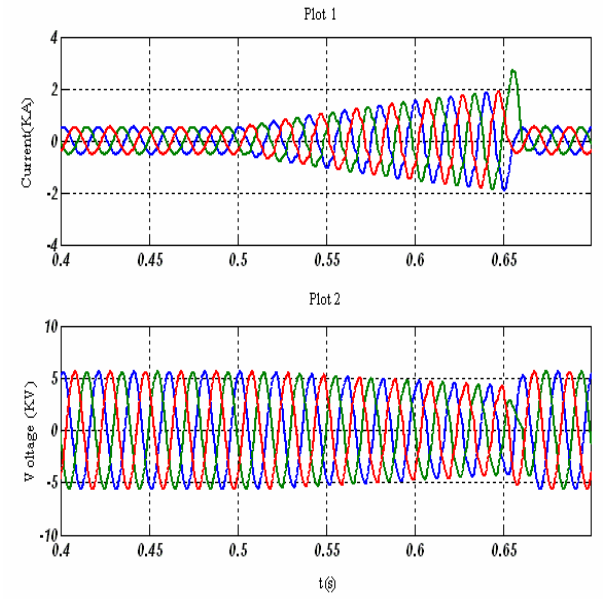



Fig. 8. Currents and voltages during fault with using FCL

By using Interline DVR-FCL system, the line current (feeder F1) as shown in plot1 of Fig.9, effectively limited by FCL port and voltage sag of PCC is compensated completely, as can be seen from plot2. Plot3 of Fig.9 shows the current of sensitive loads. Plot 1-3 from Fig.10 show the real and reactive power injected by the DVR port, the injected voltage and the capacitor voltage, respectively.

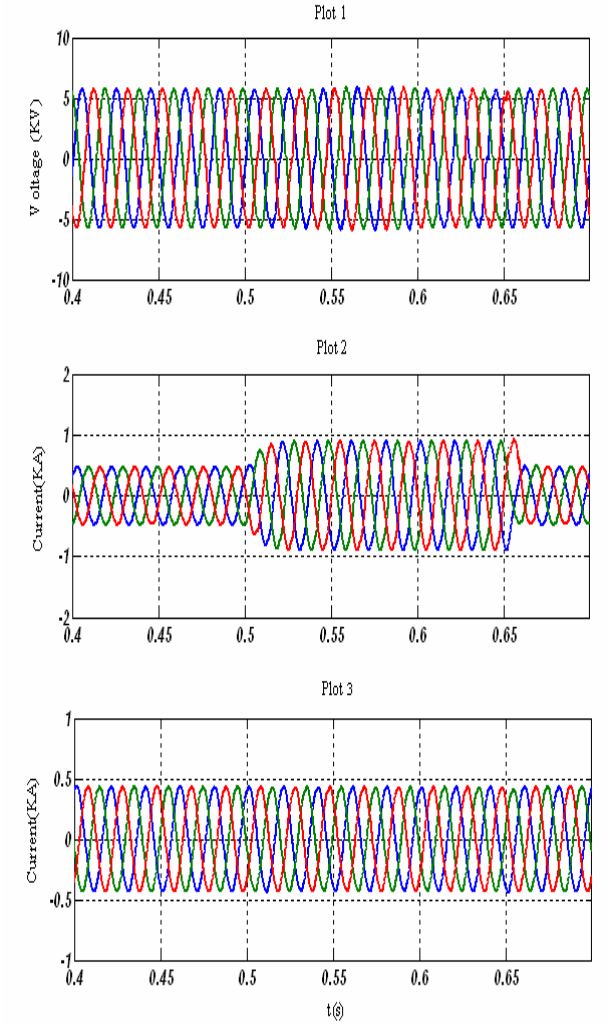
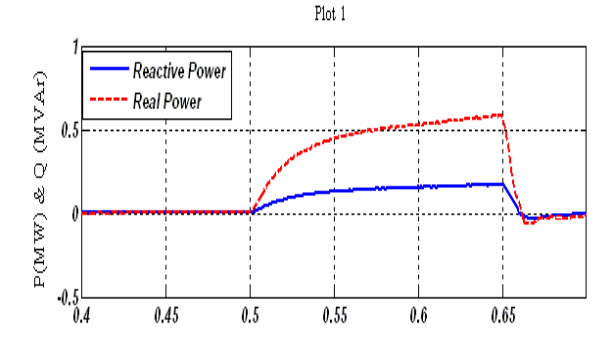



Fig.9. Currents and voltages during fault with using combined FCL- DVR



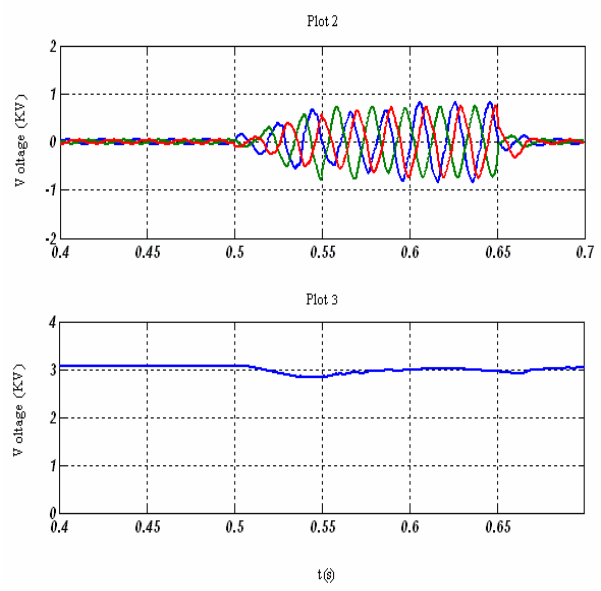



Fig.10. Response of DVR port during fault

## 6. Conclusion

In this paper a novel structure based on unique super-conducting coil is proposed which in this structure the DVR and diode bridge SFCL is combined together, for fault current limiting and power quality improving functions. The simulation results show that IDVR-FCL system not only compensates voltage sag of PCC, but also limits the peak and steady fault current with just one superconducting coil and lower rating.

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