Application of Sigma-Delta Modulation in Multifunction Current Controller for Inverter-Based Distributed Generation

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Abstract—**There are many consumers in distribution networks, which have rapid changes in the reactive power consumption. These changes can result in considerable variations in the load-side voltage and can effect the operation of other power consumers which are connected to the Point of Common Coupling (PCC). In this paper a current control strategy for Distributed Generation (DG) inverters based on Sigma Delta Modulation (SDM) is proposed. The proposed interface is called Sigma-Delta based Current Controlled Voltage Source Inverter (ΣΔ_CC_VSI), which can control the active and reactive power independently and has a fast voltage regulation. The proposed ΣΔ_CC_VSI reduces the harmonics amplitude and consequently, ElectroMagnetic Interference (EMI) problems.**

Keywords—**Active and Reactive Power Control; DG; Voltage Regulation; VSI and Sigma-Delta Modulation.**

I. INTRODUCTION

DG system is defined as an electric power source that connected directly to the distribution network or the customer.

The integration of DG systems with the utility distribution network offers a number of technical, environmental and economic benefits. It also gives a great opportunity for distribution utilities to improve the performance of networks by reducing its losses [1]. The technical challenges associated with the DG can be subdivided into three categories:

- The system interface to the grid.
- Operation and control of DG.
- Planning and design.

The subject of this paper is in the first and second category. The control system controls the active and reactive power independently. In addition, the control system aims at the fast voltage regulation of AC bus [2-3].

Voltage Source Inverter (VSI) is proposed for the interfacing between DG and distribution networks. The command signal for the VSI, which is basically a current signal, will include the information of the active power, which should be produced by DG system and reactive power, which should be injected to the system in order to control the voltage at the load-side PCC or the load reactive power. To compensate power quality problems at PCC, the current controlled VSI has been selected considering its fast dynamic, accurate performance, and its inherent closed loop current control system.

The pulse-width modulation (PWM) technique is widely used for DC/AC power inversion in particular for the uninterrupted power supply [4].

Based on this technique, it is easy to reduce harmonics and to design filters at fixed frequency. However, it is difficult to have high stability and low harmonics by PWM technique due to its open-loop control strategy.

In order to remedy the mentioned drawback, a closed-loop control Delta Modulation (DM) was proposed to generate modulation drives for the power inversion by using the feedback error signal through a hysteresis comparator [4]. In spite of precisely tracking the reference signal, the DM control always produces almost fixed harmonic distortion with low amplitude in low-order harmonics, when operating in wider frequency range. However, the frequency of the modulating signal could not be fixed and is subject to the slope of the DM feedback signal (triangular). It will then distort the harmonic spectrum and results in phase shift in the output signal after demodulation. To solve the mentioned phase-shift problem, power conversions strategy based on Sigma-Delta Modulation (SDM) is proposed [4].

In power electronics systems, attention was attracted to SDM when resonant dc link inverters had been discussed [5-6]. Even before that, Delta Modulation based current-regulators, which follow a similar principle of operation and have a very similar performance, were proposed for conventional voltage source inverters [7-8]. A profound performance analysis of SDM controlled inverters, plus approximations for some space-vector based varieties, was reported in [9-10].

The most important characteristics of SDM and related strategies are:

- Switching instants of the devices (on or off) are synchronized to a clock with frequency f_c,
- Variable switching frequency, at maximum half of the clock frequency $f_c/2$,
- Widespread output spectra with some content of low-order and sub-harmonics,
- Very simple implementation with only a few digital or analog-digital components.

In general with PWM scheme, noise peak spectra appears at every whole number of carrier frequency and this property causes bad influence on the electronic information, telecommunication and medical equipments which are abundantly fed in distribution networks [11-13].

Due to aforementioned points, SDM or DM is widely used as a modulator or controller (like in sliding mode control [14]) for power electronics devices, e.g. in power factor corrections [15], inverters [16] and DC/DC converters [17].

According to mentioned advantages, it seems that application of SDM (or DM) based inverters as an interface for DG system is useful. Thus, this paper proposes a current control strategy for VSI which separates the active and reactive power control and uses the SDM strategy as current control loop. The proposed interface for DG systems is called ΣΔ based Current Controlled Voltage Source Inverter (ΣΔ_CC_VSI). The operation of the proposed control system is simulated by PSCAD/EMTDC and its results have been compared and verified with the results of [3]. It is shown that the proposed current control strategy can reduce the harmonics of the output voltage of VSI better than the method proposed in [3].

II. Proposed Current Control Strategy

Fig. 1 shows the proposed current control strategy associated and its control blocks for a typical distribution system. The components of the system are: shunt converter, DG source, rectifier, smoothing capacitor C, transformer and current smoothing filter.

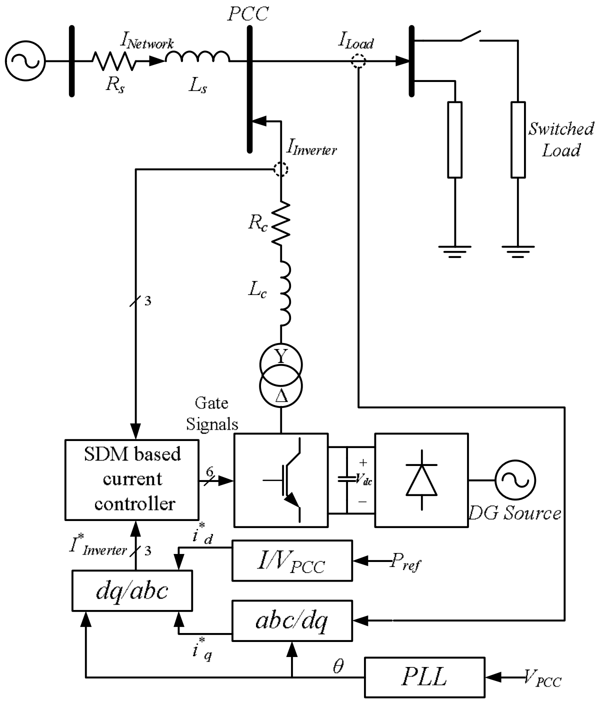


Fig. 1. Diagram of proposed ΣΔ_CC_VSI

The converter manages the amount of $I_{Inverter}$ injected to the PCC bus. The load current, I_L is converted from the three phase coordinates to the synchronously rotating frame by using equation (1), where θ is the instantaneous angle of the PCC voltage vector, obtained from Phase Locked Loop (PLL) circuit.

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} \cos(\theta) & \cos(\theta - 2\pi/3) & \cos(\theta + 2\pi/3) \\ -\sin(\theta) & -\sin(\theta - 2\pi/3) & -\sin(\theta + 2\pi/3) \\ \sqrt{1/2} & \sqrt{1/2} & \sqrt{1/2} \end{bmatrix} \times \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \qquad (1)$$

The PLL system is shown in more detailed Fig. 2.

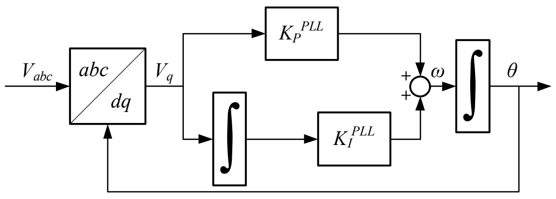


Fig. 2. Block diagram of PLL

In this paper, it is assumed that there is no path for the zero sequence components, therefore i_0 in (1) and v_0 in Fig. 2 can be ignored. However, these variables have been considered in the formulation to present the general case.

The adjustment of the *dq*-transformation is so that the voltage at the PCC has no *q*-axis component [18]. A PI regulator controls the angular frequency by (2). Then the transformation angle can be determined by (3).

$$\omega = K_P^{PLL} v_q + K_I^{PLL} \int (v_q \times dt) \qquad (2)$$

$$\theta = \int (\omega \times dt) \qquad (3)$$

The resultant *q*-component is responsible for the reactive power flow through the utility network. To compensate the reactive component using ΣΔ_CC_VSI, simply put the quadrature component (i.e., i_q^*) of the reference current of VSI, $I_{Inverter}^*$, equal to the quadrature component (i.e., i_{lq}) of the load current (I_{Load}) as follows:

$$i_q^* = i_{lq} \qquad (4)$$

Considering the capacity of the reactive power generation of DG and the size of VSI, a limiter can be used for i_{lq}, to ensure that i_q^* is in the permissible range. The generated active power of DG is expressed by the following equation:

$$P = v_d \times i_d + v_q \times i_q \qquad (5)$$

Where v_d and v_q are the *dq* components of the PCC voltage (V_{PCC}) in the synchronously rotating frame, respectively and i_d and i_q are the *dq* component of the three phase DG current, $I_{Inverter}$. As mentioned before, we have:

$$v_d = V_{PCC} \quad \text{and} \quad v_q = 0 \qquad (6)$$

Substituting equation (4) into (5) yields:

$$i_d = P / V_{PCC} \qquad (7)$$

Selecting the reference active power of DG as the command signal given of the utility the equation (6) can be rewritten, as follows:

$$i_d^* = \frac{P_{ref}}{V_{PCC}} \qquad (8)$$

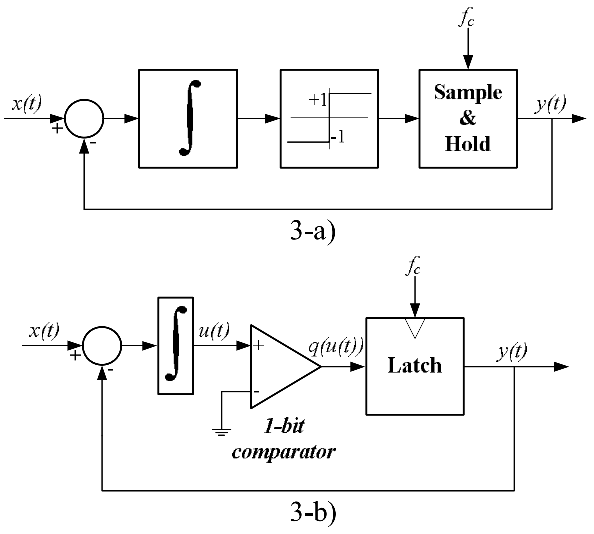
Where i_d^* is the direct component of the reference current of the VSI, $I_{Inverter}^*$. This component is also responsible for the losses in both the converter and the capacitor. Finally, applying inverse *dq* transformation rotating at the supply frequency ω by the equation (9), the three phases VSI reference currents are determined from the *dq* reference components.

$$\begin{bmatrix} i_{ac}^* \\ i_{bc}^* \\ i_{cc}^* \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} \cos(\theta) & -\sin(\theta) & \sqrt{1/2} \\ \cos(\theta - 2\pi/3) & -\sin(\theta - 2\pi/3) & \sqrt{1/2} \\ \cos(\theta + 2\pi/3) & -\sin(\theta + 2\pi/3) & \sqrt{1/2} \end{bmatrix} \qquad (9)$$
$$\times \begin{bmatrix} i_d^* \\ i_q^* \\ i_0^* \end{bmatrix}$$

The reactive and active power are decoupled through ΣΔ_CC_VSI by this simple control scheme. Note that the power exchanged by the ΣΔ_CC_VSI is limited by the DG energy capacity.

III. SDM TECHNIQUE APPLIED TO ΣΔ_CC_VSI

As shown in Fig. 3-a, the SDM is a unity feedback system with an integrator and comparator in the forward path. The output, and also the feedback, is a two-level digital signal $v_o = \pm V_o$ [17].



3-a)

3-b)

Fig. 3. SDM a) Block diagram b) equivalent circuit

A delta modulator or sigma-delta modulator converts a continuous analog signal into a digital pulse train and is most commonly used for telecommunication of speech [17]. When applied to inverter control (Fig. 4), the inverter and motor are equivalent to the transmission medium and demodulator of the telecommunication system. A SDM is chosen because the standard SDM is a first-order low-pass filter, which, with a good approximation, is the frequency response of an induction motor or inverter filter.

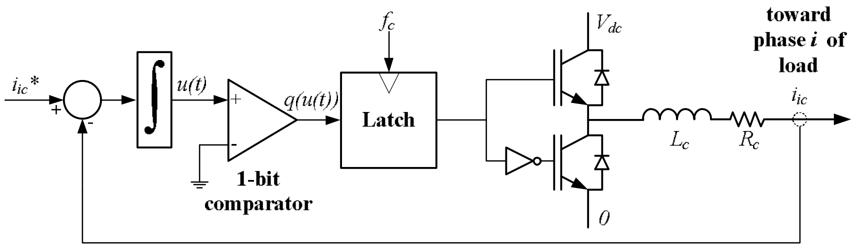


Fig. 4. ΣΔ Current Controller technique (inverter embedded in SDM loop)

SDM is categorized in the category with the simplest form, shown in Fig. 3 [17]. *x* is the input signal, *u* is the integrator state, and *y* is the latch output. The comparator is a quantizer whose output, *q(u)* is ±1 according to the sign of the integrator state *(u)*. The latch samples the comparator or quantizer output *q(u)* at the sampling frequency f_c and holds that value until the next sampling instant.

The SDM uses feedback to lock onto a band-limited input signal *x(t)*. As explained in [19], "Unless the input signal *x(t)* exactly equals one of the discrete quantizer output levels, a tracking error results. The integrator accumulates the tracking error over time and the quantizer and latch feedback a value that will minimize the accumulated tracking error. Thus, the quantizer output *y(t)* toggles about the input signal *x(t)* so that the average quantizer output is approximately equal to the average of the input."

To illustrate how a power electronic circuit can be embedded in a SDM, consider the modulator for the half bridge converter shown in Fig. 4. In this arrangement the gating circuitry and half-bridge are embedded into the loop following the latch in Fig. 3-b. The comparator and latch set the switch state for each sampling period according to the sign of the comparator input *(u)* at the sampling instant. The switch state impresses the voltage $\pm V_o$ on the output, *y(t)*. Since figures 3 and 4 are different implementations of the same overall quantizing and latch functions, the corresponding modulators have identical behavior. Thus, assuming the input signal *x(t)* to be the desired output voltage, the actual output voltage *y(t)* will be approximately the desired output voltage. In the next section it is shown that, this approximation can be improved by the generalization of the integrator in Fig. 3 to a linear filter or by increasing the sampling rate f_c.

IV. SIMULATION RESULTS

The performance of the proposed ΣΔ_CC_VSI is studied by the simulations using PSCAD/EMTDC program. The parameters of the system under study have been given in the appendix of [3] and EMTDC time step has been set at 10 (µsec). In addition, the sampling rate (f_c) has been set at 20 (kHz). The following simulation results illustrate the operation of ΣΔ_CC_VSI in reactive power compensation at the PCC under sudden load change, and setting the active power at its reference value. Fig. 5, shows the dynamic response of the proposed ΣΔ_CC_VSI. The load of 1.1 (p.u.) is switched at t = 0.2 (sec), and then removed at t = 0.4 (sec), as shown in Fig. 5-a. It is clear from Fig. 5-b that the ΣΔ_CC_VSI succeeded in tracking and compensating the reactive power demand of the load with fast dynamics and with minimum overshoot. Fig. 5-c shows that the active power to ΣΔ_CC_VSI is almost constant and equal to its input command value (17 kW). Considering from Fig. 5-b and 5-c it can be said that the control of the active and reactive power is decoupled.

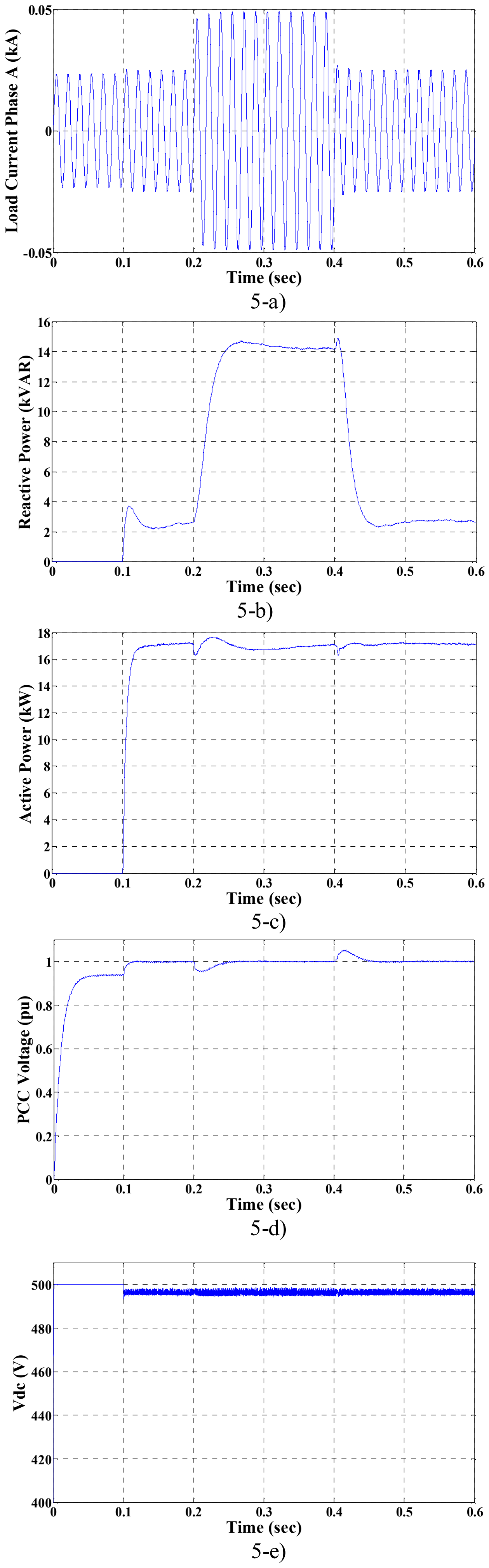
In addition, Fig. 5-d shows the effect of ΣΔ_CC_VSI on the PCC voltage. ΣΔ_CC_VSI has improved the per unit voltage at PCC from 0.9 (p.u.) to 1.0 (p.u.). Finally, Fig. 5-e shows the DC bus voltage, which is obviously constant.

The second simulation wants to evaluate the internal performance of the ΣΔ based VSI. Fig. 6 and 7 present two windows of Fig. 5, in the period of load changes. Fig. 6-a shows the phase voltage at PCC, (V_{sa}), Fig. 6-b shows the network current ($I_{Network\text{-}a}$) and load current ($I_{Load\text{-}a}$) and Fig. 6-c shows the quadrature component (i.e., i_q^*) of the inverter current under dynamic changes of the load reactive power. The control strategy for generating i_q^* is based on voltage controlling. So, the measured RMS per-unit voltage is compared with the 1 (p.u.) and the difference (control signal) is passed through the Proportional-Integral (PI) controller to produce the reference current.

It is clear that the network current is without overcurrent and with smooth transition. Here the power command for the ΣΔ_CC_VSI was set equal to the load power (17kW). Therefore, there is no current fed to the load from the utility, the load nearly takes its power from DG. When the load increases, the amount of increment in active power is drawn from the utility, while the ΣΔ_CC_VSI still compensate reactive power. Fig. 6-d shows the VSI current of phase A used ΣΔ Current Controller (ΣΔ_CC). Fig. 6-e is the same as Fig. 6-d, but in this figure the load is disconnected. The value of THD for PCC voltage and ΣΔ_CC_VSI current are 1.5% and 1%, respectively which both are smaller than results of [3].

ΣΔ_CC in nature is a closed loop control which is described in section III. According to section III, the ΣΔ_CC leads to the fast dynamic response and in comparison with Hysteresis Current Control (HCC used in [3]) has lower harmonic for voltage before filtering and lower THD for current and voltage, too. Fig. 7 shows the third and fifth harmonics of the phase voltage versus time. As shown in Fig. 7, in ΣΔ_CC technique the amplitude of the third and fifth harmonics is almost constant even with suddenly load changes.

As a result, the ΣΔ_CC technique has faster response than HCC technique. The ΣΔ_CC technique can keep the amplitude of harmonics constant based on the noise shaping property of SDM [17]. Note that, the variations of unfiltered voltage harmonics amplitude can cause EMI problems. The sampling frequency of the sample and hold block, f_c, directly controls the amount of ripples in the output current of the VSI. The switching frequency is changed by the sampling frequency of the sample and hold block.



5-a)

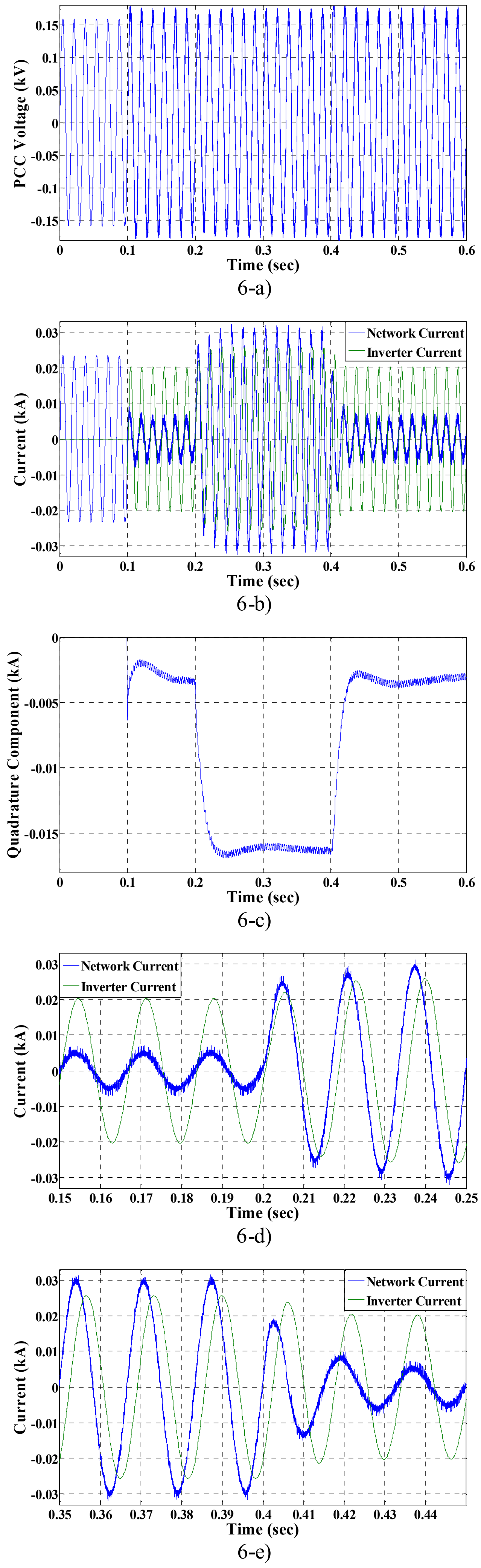
5-b)

5-c)

5-d)

5-e)

Fig. 5. Dynamic response of proposed ΣΔ_CC_VSI due to sudden load change a) load current b) reactive power variations c) reactive power variations d) VPCC variations and e) DC bus voltage



6-a)

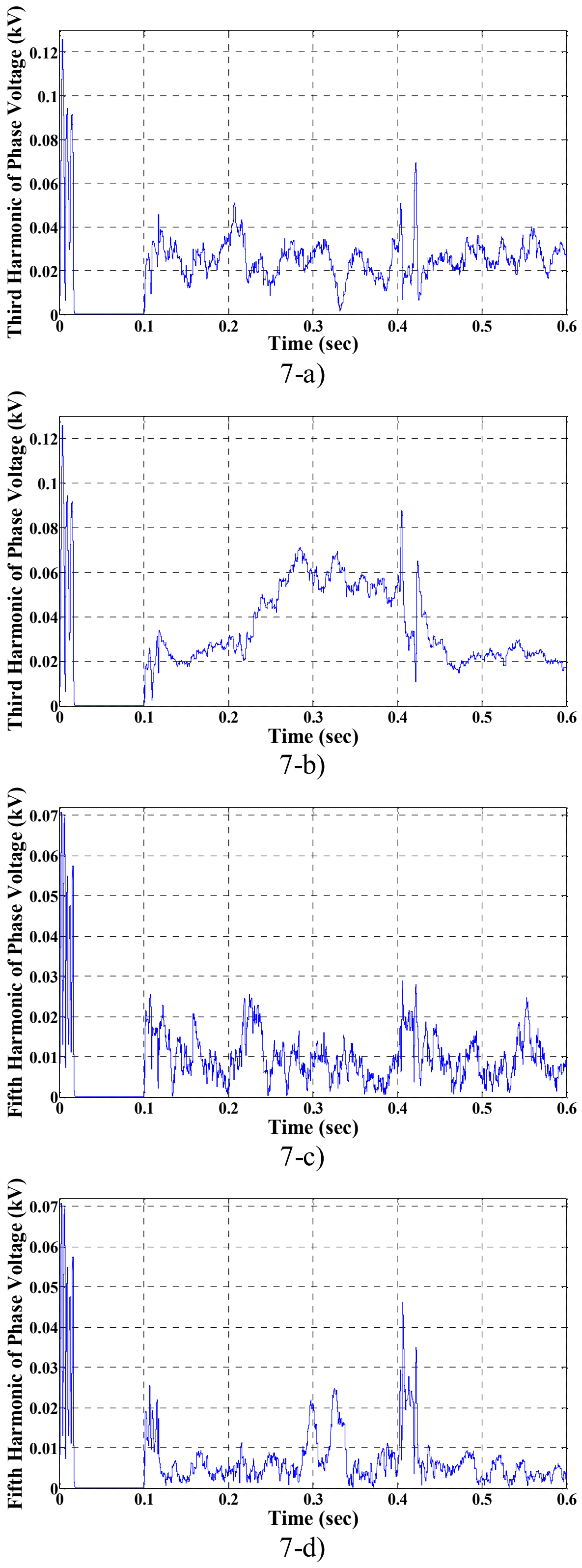
6-b)

6-c)

6-d)

6-e)

Fig. 6. Current variations in ΣΔ_CC_VS a) voltage phase A at PCC b) network and inverter current c) quadrature component of inverter current d) enlargement of Fig. 6-b) between t=0.15 (sec) to t=0.25 (sec) e) enlargement of Fig. 6-b) between t=0.35 (sec) to t=0.45 (sec)



7-a)

7-b)

7-c)

7-d)

Fig. 7. Harmonics of phase voltage in VSI a) third harmonic with ΣΔ_CC technique b) third harmonic with HCC technique c) fifth harmonic with ΣΔ_CC technique d) fifth harmonic with HCC technique

V. CONCLUSION

DG systems and distributed networks have many consumers and equipments which have rapid changes in the reactive power consumption. These changes can cause considerable variations of the load-side and PCC voltage.

In this paper, to overcome the power quality problems at PCC, current controlled VSI has been selected considering, its fast dynamic response, accurate performance, ease of implementation and its inherent closed loop control. A current control strategy for inverters interfacing in DG has been proposed based on SDM, too.

The proposed interface (ΣΔ_CC_VSI) controls the active and reactive power independently with fast dynamic response. The proposed ΣΔ_CC_VSI reduced the harmonics amplitude variations of the unfiltered voltage and THD of voltage and current. Therefore, it reduces the

EMI side effects, which is important for distribution system sensitive consumers like medical equipments.

The simulation results have been shown that the proposed inverter interface has multifunction operation. Because there is no requirement for the active power filter to compensate the reactive power and it has fast voltage regulation. In addition, the proposed inverter interface provides the active power requirement of load, simultaneously.

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